



**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

Group Art Unit: 2811  
Examiner: Thomas J. Margee

**In Re PATENT APPLICATION Of:**

**Applicant:** Hiroaki NAKANO

Serial No.: 10/756,366

**Filed: January 14, 2004**

For: Circuit board for mounting a semiconductor chip)  
and manufacturing method thereof )

Attorney Ref.: TAI 146

) INFORMATION DISCLOSURE  
 ) STATEMENT

July 5, 2005

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

**Sir:**

This is an information disclosure statement submitted in compliance with the timing requirements of 37 C.F.R. §1.97 before a first Office Action on the merits, in an RCE filed on even date herewith.

Copies of four (4) documents, and a Form PTO-1449 listing the documents are submitted herewith.

Consideration of the submitted documents is respectfully requested.

Should any further fee be required, please charge the same to our Deposit Account No. 18-0002 and advise us accordingly.

Respectfully submitted,

Nick Brown

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July 5, 2005  
Date

NSB:klc

**FORM PTO-1449****INFORMATION DISCLOSURE  
STATEMENT**Atty. Docket:  
**TAI 146**Application No.:  
**10/756,366**Applicant:  
**Hiroaki NAKANO**Filing Date:  
**January 14, 2004**Group Art Unit:  
**2811****U.S. PATENT DOCUMENTS**

Examiner Initial		Document Number	Date	Name	Class	Sub-Class	Filing Date
	AA						
	AB						
	AC						
	AD						
	AE						

**FOREIGN PATENT DOCUMENTS**

		Document Number	Date	Country	Class	Sub-Class	Trans-Lation
	AF	JP-A 2001-15638	01/19/01	Japan			abstract
	AG	JP-A 11-284101	10/15/99	Japan			abstract
	AH	JP-A 2003-92376	03/28/03	Japan			abstract
	AI	JP-A 8-213741	08/20/96	Japan			abstract
	AJ						

**OTHER (Including Author, Title, Date, Pertinent Pages, etc.)**

	AK	
	AL	

Examiner

Date Considered

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.

